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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/685,863	10/15/2003	Hans M. Jacobson	YOR920030295US1 (163-9)	5806

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EXAMINER	
CHANG, DANIEL D	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 02/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/685,863	JACOBSON ET AL.	
	Examiner	Art Unit	
	Daniel D. Chang	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-57* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9-12,14,16,17,20-22,26,27,29,31-38,40-43,45,47,48 and 51-56* is/are rejected.

7)☒ Claim(s) *8, 15, 18, 19, 23-25, 28, 30, 39, 44, 46, 49, 50, and 57* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Objections

Claim 39 is objected to because of the following informalities: claim 39 is depending itself. It appears that claim 39 be depending from claim 38. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 10, 36, and 54 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted elements are: the cooperative relationship between the pulse wave and a clock cycle time.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-7, 9, 11-12, 14, 16-17, 20-22, 26-27, 29, 31-35, 37-38, 40-43, 45, 47-48, 51-53, and 55-56 are rejected under 35 U.S.C. 102(b) as being anticipated by Kumagai et al. (US 6,208,171 B1).

Regarding claim 1, Kumagai discloses, at least in Fig. 11, a leakage current control device, comprising:

a circuit (33) having one or more functions in a data path (S) where the functions are executed in a sequence, each of the functions having power reduction logic (31, 32) to selectively energize each respective function; and

a leakage control circuit (CS CONTROL CKT), which interacts with the power reduction logic, so that the functions are energized or deenergized in a control sequence (col. 11, lines 5+) such the functions where the data is resident are energized and at least one of the other functions is not energized (col. 11, lines 60+).

Regarding claims 2 and 3, Kumagai discloses, at least in Fig. 11, that the circuit includes a pipeline (33(n-1), 33(n), 33(n+1)) and the functions include combinational logic (NOR, NAND gates) in a pipeline stage.

Regarding claim 4, Kumagai discloses, at least in Fig. 11, that the circuit includes a pipeline (33(n-1), 33(n), 33(n+1)) and the functions include sequential logic (Input Latch in Fig. 15) in a pipeline stage.

Regarding claim 5, Kumagai discloses, at least in Fig. 11, that the circuit includes a pipeline (33(n-1), 33(n), 33(n+1)) and tile functions (Logical CKTS) are included in one or more stages of the pipeline.

Regarding claim 6, Kumagai discloses, at least in Fig. 11, that the power reduction logic is divided into individually enabled portions (CSB(n-1)-CSB(n+1), CS(n-1)-CS(n+1)), each portion being enabled in accordance with the control sequence (ICB, IC).

Regarding claim 7, Kumagai discloses, at least in Fig. 11, that the power reduction logic (31, 32) is divided into individually enabled portions, each portion having a threshold voltage

adjusted for transistors (PFET and NFET in 31, 32) within each respective portion in accordance with the control sequence.

Regarding claim 9, Kumagai discloses, at least in Fig. 11, that the power reduction logic (31, 32) is energized in accordance with a pulse wave (CSB, CS).

Regarding claim 11, Kumagai discloses, at least in Fig. 11, that the power reduction logic is energized in accordance with a front edge of a pulse wave (when CSB goes high) and at least partially deenergized in accordance with a back edge of the pulse wave (when CSB goes low).

Regarding claim 12, Kumagai discloses, at least in Fig. 11, that the power reduction logic (31, 32) is divided into individually enabled portions such that only a subset of the portions are energized at a time (col. 11, lines 60+).

Regarding claim 14, Kumagai discloses, at least in Fig. 11, that the leakage control circuit selectively employs retentive (when PFET and NFET in 31 and 32 are OFF) and non-retentive means (when PFET and NFET in 31 and 32 are ON) to reduce current leakage.

Regarding claim 16, Kumagai discloses, at least in Fig. 11, that the retentive means includes partial supply voltage (VVD, VGD) and/or ground gating.

Regarding claim 17, Kumagai discloses, at least in Fig. 11, that the non-retentive means includes supply voltage (VDD, GND) and/or ground gating.

Regarding claim 20, as for the recitation, "the device is employed in a system", it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex parte Masham, 2 USPQ2d 1647 (1987).

Regarding claim 21, Kumagai discloses, at least in Fig. 11, that individual components of the subunit (33) are controlled at a component level by the leakage control circuit (31, 32) to selectively control power.

Claims 22, 26-27, 29, 31-35, 37-38, 40-43, 45, 47-48, 51-53, and 55-56 are essentially the same in scope as apparatus claims 1-7, 9, 11-12, 14, 16-17, and 20-21 and are rejected similarly.

Allowable Subject Matter

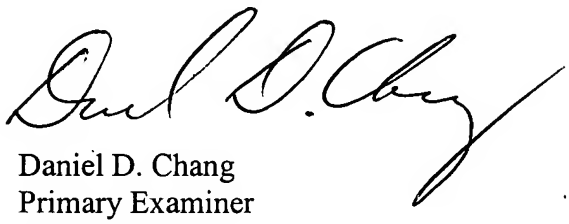
Claims 8, 15, 18, 19, 23-25, 28, 30,39, 44, 46, 49, 50, and 57 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel D. Chang whose telephone number is (571) 272-1801. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J. Tokar can be reached on (571) 272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Daniel D. Chang
Primary Examiner
Art Unit 2819

dc

DANIEL CHANG
PRIMARY EXAMINER